

What is claimed is:

1. A method for fabricating a semiconductor memory device, comprising steps of:

depositing first and second insulating layers on a semiconductor substrate where a shallow trench isolation (STI) region and a deep trench isolation (DTI) region are defined;

forming the STI region by selectively etching the second and first insulating layers and the semiconductor substrate;

forming a photoresist to cover the STI region and curing the surface of the photoresist; and

forming the DTI region by using the cured photoresist and the second insulating layer as a mask.

2. The method according to claim 1, wherein the curing step of the photoresist surface includes implanting high energy argon ions into the photoresist.

3. The method according to claim 2, wherein implanting concentration of the argon ions is 10^{12-15}cm^{-3} and the implanting energy is 10~200KeV.

4. The method according to claim 1, wherein the curing step of the photoresist surface is performed by e-beam curing process.

5. The method according to claim 4, wherein the energy of the e-beam curing process is $1000\sim 2000\text{uC}/\text{cm}^2$.

6. The method according to claim 1, wherein the photoresist formation process includes exposure process, which selects one light source among i-ray (365nm), KrF(248nm) and ArF(193nm).

7. The method according to claim 1, wherein the first insulating layer is a pad oxide layer.

8. The method according to claim 1, wherein the second insulating layer is a pad nitride layer.

9. The method according to claim 1, wherein the STI region has a depth of $2500\sim 3000\text{\AA}$ from the surface of the semiconductor substrate.

10. The method according to claim 1, wherein the

DTI region has a depth of 7000~8000Å from the surface
of the semiconductor surface.

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of the semiconductor surface.